Amendments to the Claims:

1. (Currently Amended) A method for use in connection with an integrated circuit design, the method comprising:

identifying distinct timing paths of the integrated circuit design, the distinct timing paths having timing violations;

identifying a first subset of the distinct timing paths including a plurality of timing paths wherein each of the plurality of timing paths includes at least one first common characteristic;

within the plurality of timing paths forming the first subset, grouping the timing paths into one or more groups, each timing path within a group having at least one second common characteristic,

correcting a first timing path violation for one of the timing paths within the group; [[and]]

repeating the first timing path violation correction for at least one of the other timing paths within the group; and

identifying a second subset of the distinct timing paths including a second plurality of timing paths, wherein each of the second plurality of timing paths includes at least one third common characteristic, wherein a particular timing path including the at least one first characteristic and the at least one third characteristic is identified with a subset based on a prioritization of the first subset and the second subset, wherein the prioritization is based at least in part on the number of groups within each subset.

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2. (Previously Presented) The method, as recited in claim 1, wherein the second common characteristic is a sequence of devices.

3-4. (Cancelled)

5. (Previously Presented) The method, as recited in claim 1, wherein the grouping further includes forming one or more other groups, each timing path within the other groups being a common portion of a timing path of the other groups, and having a common sequence of device elements.

6. (Previously Presented) The method, as recited in claim 1, wherein the first common characteristic comprises an origin of a timing path.

7. (Previously Presented) The method, as recited in claim 1, wherein the first common characteristic comprises a destination of a timing path.

8. (Previously Presented) The method, as recited in claim 1, wherein the first common characteristic comprises inclusion of a first block in a timing path.

9. (Previously Presented) The method, as recited in claim 1, wherein the first common characteristic comprises inclusion of a first net in a timing path.

10. (Previously Presented) The method, as recited in claim 1, wherein correcting a first timing path violation includes reducing a maximum timing violation.

11. (Previously Presented) The method, as recited in claim 1, wherein correcting a first timing path violation includes reducing a minimum timing violation

12. (Previously Presented) The method of claim 1, further comprising:

substituting in the integrated circuit design, a plurality of replacement circuits, each one of the plurality of replacement circuits corresponding to a respective timing path of the group, the plurality of circuits based at least in part on the correction of the first timing path violation.

13. (Previously Presented) The method of claim 12, further comprising: fabricating an integrated circuit including the plurality of replacement circuits.

14. (Previously Presented) The method of claim 1, further comprising: preparing the integrated circuit design and thereafter performing the correcting and repeating.

15. (Previously Presented) A semiconductor integrated circuit manufactured using the method of claim 1.

16-22. (Cancelled)

23. (Previously Presented) The method of claim 1 further comprising making a computer readable encoding of the semiconductor integrated circuit design, wherein the computer readable encoding is stored on a computer readable medium.

24-26. (Cancelled)

27. (Previously Presented) The method of claim 1 further comprising:

preparing one or more design files for the semiconductor integrated circuit design.

28-30. (Cancelled)

31. (Currently Amended) An article of manufacture comprising:

a computer usable medium having computer readable instructions embodied therein to cause a machine to perform operations including:

identifying distinct timing paths of the integrated circuit design, the distinct timing paths having timing violations;

identifying a first subset of the distinct timing paths including a plurality of timing paths wherein each of the plurality of timing paths includes at least one first common characteristic;

within the plurality of timing paths forming the first subset, grouping the timing paths into one or more groups, each timing path within a group having at least one second common characteristic being a sequence of devices;

correcting a first timing path violation for one of the timing paths within the group; [[and]]

repeating the first timing path violation correction for at least one of the other timing paths within the group; and

identifying a second subset of the distinct timing paths including a second plurality of timing paths including at least one third common characteristic, wherein a particular timing path including the at least one first characteristic and the at least one third characteristic is identified with a subset based on a prioritization of the first subset and the second subset.

32-35. (Cancelled)

36. (Currently Amended) An apparatus comprising:

means for identifying distinct timing paths of an integrated circuit design, the distinct timing paths having timing violations;

means for identifying a first subset of the distinct timing paths including a plurality of timing paths wherein each of the plurality of timing paths includes at least one first common characteristic;

within the plurality of timing paths forming the first subset, means for grouping the timing paths into one or more groups, each timing path within a group having at least one second common characteristic[[,]] ;

means for correcting a first timing path violation for one of the timing paths within the group; [[and]]

means for repeating the first timing path violation correction for at least one of the other timing paths within the group; and

means for identifying a second subset of the distinct timing paths including a second plurality of timing paths, wherein each of the second plurality of timing paths includes at least one third common characteristic, wherein a particular timing path including the at least one first characteristic and the at least one third characteristic is identified with a subset based on a prioritization of the first subset and the second subset, wherein the prioritization is based at least in part on the number of groups within each subset.

37. (Previously Presented) The apparatus as recited in claim 36, further comprising:

means for substituting in the integrated circuit design, a plurality of replacement circuits, each one of the plurality of replacement circuits corresponding to a respective timing path of the group, the plurality of circuits based at least in part on the means for correcting a first timing path violation.

38. (Previously Presented) The method of claim 1 wherein the correcting a first timing path violation comprises inserting at least one circuit element.